Claims

1. A method for forming a buried cavity in a semiconductor substrate formed by at least a first wafer and a second wafer both of semiconductor material directly bonded along a bond interface, the method comprising the steps of:

treating one of the first and second wafers to be selectively etchable adjacent a surface thereof to form a selectively etchable portion prior to bonding of the first and second wafers,

bonding the first and second wafers together with the surface of the one of the first and second wafers adjacent which the portion of the wafer is selectively etchable forming with a surface of the other of the first and second wafers the bond interface,

forming a communicating opening through the first wafer to the selectively etchable portion, and

etching the selectively etchable portion to form the buried cavity beneath the first wafer.

2. A method as claimed in Claim 1 in which the one of the first and second wafers which is treated to be selectively etchable is treated through the surface thereof which is to form the bond interface.

3. A method as claimed in Claim 1 in which the one of the first and second wafers which is treated to be selectively etchable is treated by doping.

4. A method as claimed in Claim 3 in which the one of the first and second wafers which is treated to be selectively etchable is doped by ion implantation through the surface which is to form the bond interface.

5. A method as claimed in Claim 3 in which the one of the first and second wafers which is treated to be selectively etchable is doped by atom diffusion through the surface which is to form the bond interface.

6. A method as claimed in Claim 3 in which the one of the first and second

wafers which is treated to be selectively etchable is of p type material, and the wafer is doped to form the selectively etchable portion as a p+ region.

7. A method as claimed in Claim 6 in which the one of the first and second wafers which is to be treated to be selectively etchable is doped by boron, or species thereof.

8. A method as claimed in Claim 3 in which the one of the first and second wafers which is treated to be selectively etchable is of n type material, and the wafer is doped to form the selectively etchable portion as a n+ region.

9. A method as claimed in Claim 8 in which the one of the first and second wafers which is treated to be selectively etchable is doped by a dopant selected from one or more of the following dopants:

phosphorous,
arsenic, and
antimony,
or species thereof.

10. A method as claimed in Claim 3 in which the one of the first and second wafers which is treated to be selectively etchable is doped at a level greater than 10^{18} atoms per cc.

11. A method as claimed in Claim 1 in which the one of the first and second wafers which is treated to be selectively etchable is treated so that the depth of the selectively etchable portion corresponds to the desired depth of the buried cavity.

12. A method as claimed in Claim 1 in which the one of the first and second wafers which is treated to be selectively etchable is treated so that the area of the selectively etchable portion corresponds to the desired area of the buried cavity.

13. A method as claimed in Claim 1 in which the one of the first and second

wafers which is treated to be selectively etchable is treated so that the area of the selectively etchable portion extends substantially over the entire bond interface.

14. A method as claimed in Claim 1 in which the second wafer is treated to be selectively etchable in its entirety, and a third wafer of semiconductor material is bonded to the second wafer so that the second wafer is sandwiched between the third wafer and the first wafer.

15. A method as claimed in Claim 14 in which the third wafer is directly bonded to the first wafer.

16. A method as claimed in Claim 1 in which the second wafer is treated to be selectively etchable.

17. A method as claimed in Claim 1 in which the first wafer is treated to be selectively etchable.

18. A method as claimed in Claim 1 in which the first and the second wafer are treated to be selectively etchable, and the first and second wafers are bonded together with their respective surfaces which are adjacent the portions thereof which are selectively etchable forming the bond interface.

19. A method as claimed in Claim 1 in which the selectively etchable portion is etched by a wet etch to form the buried cavity.

20. A method as claimed in Claim 1 in which the communicating opening is formed in the first wafer by etching.

21. A method as claimed in Claim 20 in which the communicating opening is etched in the first wafer by a reactive ion etch (RIE).

22. A method as claimed in Claim 1 in which an etch stop is formed in the

selectively etchable portion for defining the area of the buried cavity prior to etching of the selectively etchable portion for limiting the etch in a lateral direction to form the buried cavity.

23. A method as claimed in Claim 22 in which the etch stop is formed in the selectively etchable portion after bonding of the wafers.

24. A method as claimed in Claim 23 in which an etch stop forming trench is formed through one of the wafers into the selectively etchable portion, and an etch stop material is located in at least the portion of the etch stop forming trench in the selectively etchable portion for forming the etch stop.

25. A method as claimed in Claim 24 in which the etch stop forming trench is formed by etching.

26. A method as claimed in Claim 24 in which the etch stop forming trench is etched by an RIE etch.

27. A method as claimed in Claim 24 in which the etch stop forming trench is formed in the first wafer.

28. A method as claimed in Claim 1 in which the communicating opening is formed in the first wafer adjacent the centre of the area of the first wafer which is to be above the buried cavity, and the buried cavity is formed radiating laterally outwardly from and around the communicating opening.

29. A method as claimed in Claim 1 in which a pair of communicating openings are formed in the first wafer spaced apart from each other.

30. A method as claimed in Claim 1 in which the buried cavity is at least partially filled with an electrically insulating material for forming a buried insulating layer beneath the first wafer for forming with a portion of the first wafer above the buried

insulating layer a semiconductor-on-insulator (SOI).

31. A method as claimed in Claim 30 in which the electrically insulating material with which the buried cavity is at least partially filled is an oxide.

32. A method as claimed in Claim 30 in which the electrically insulating material with which the buried cavity is at least partially filled is deposited in the buried cavity.

33. A method as claimed in Claim 30 in which the electrically insulating material with which the buried cavity is at least partially filled is grown in the buried cavity.

34. A method as claimed in Claim 1 in which an electrical isolation trench is formed in the first wafer for electrically isolating an area of the first wafer above the buried cavity.

35. A method as claimed in Claim 34 in which the electrical isolation trench is at least partly filled with an electrically insulating material.

36. A method as claimed in Claim 34 in which the communicating opening is located to form a part of the electrical isolation trench.

37. A method as claimed in Claim 36 in which the portion of the electrical isolation trench which is not formed by the communicating opening, is formed after filling of the buried cavity with the electrically insulating material.

38. A method as claimed in Claim 1 in which each communicating opening is at least partially filled with an electrically insulating material.

39. A method as claimed in Claim 1 in which each communicating opening is filled with an electrically insulating material.

40. A method as claimed in Claim 1 in which each communicating opening is at

least partially filled with polysilicon.

41. A method as claimed in Claim 1 in which each communicating opening is filled with polysilicon.

42. A method as claimed in Claim 1 in which a plurality of discrete buried cavities are formed in the semiconductor substrate.

43. A method as claimed in Claim 42 in which at least some of the buried cavities are at least partially filled with the electrical insulating material for forming a plurality of discrete SOIs.

44. A method as claimed in Claim 1 in which the first wafer is thinned after the buried cavity has been formed.

45. A method as claimed in Claim 1 in which each wafer is of single crystal silicon material.

46. A semiconductor substrate having a buried cavity therein, the semiconductor substrate being formed by the method as claimed in Claim 1.

47. A semiconductor substrate having an SOI formed therein, the SOI being formed by the method as claimed in Claim 30.

48. A semiconductor substrate having a buried cavity therein, the semiconductor substrate comprising:

a first wafer of semiconductor material,

a second wafer of semiconductor material directly bonded to the first wafer along a bond interface,

one of the first and second wafers having been treated to form a selectively etchable portion adjacent a surface thereof prior to bonding of the first and second wafers, and

the buried cavity having been etched in the selectively etchable portion beneath the first wafer through a communicating opening formed in the first wafer.

49. A semiconductor substrate having an SOI formed therein, the substrate comprising:

a first wafer of semiconductor material,

a second wafer of semiconductor material directly bonded to the first wafer along a bond interface,

one of the first and second wafers having been treated to form a selectively etchable portion adjacent a surface thereof prior to bonding of the first and second wafers,

a buried cavity having been etched in the selectively etchable portion beneath the first wafer through a communicating opening formed in the first wafer, and

an electrically insulating layer formed in the buried cavity for forming with a portion of the first wafer above the buried insulating layer the SOI.